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com
if the DRAM is determined to be operating in the full density mode, refreshing the DRAM at a first rate; and

if the DRAM is determined to be operating in the reduced density mode, refreshing the DRAM at a second rate, the second rate being 8 times slower than the first rate.

REMARKS

Claims 11-14, 27-29, 36-38, 42 in 43 have been presented for examination. Claim 42 has been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,104,641 to Itou. Claims 11, 12 and 14 have been rejected under 35 U.S.C. § 103(a) as being obvious over the patent to Itou. Claims 27, 28, 36 and 37 have been rejected as being obvious over U.S. Patent No. 6,044,029 to Shore in view of the patent to Itou. Claims 13, 29, 38 and 43 have been objected to as being dependent upon a rejected base claim but are otherwise considered to be allowable.

Applicants are hereby amending all of the allowable claims to place them in condition for allowance. Specifically, claim 12 is being amended to add the subject matter of allowable claim 13, claim 27 is being amended to add the subject matter of allowable claim 29, claim 36 is being amended to add the subject matter of allowable claim 38, and claim 42 is being amended to add the subject matter of allowable claim 43. Finally, the allowable claims that have been incorporated into rejected claims to make them allowable have been cancelled.

Insofar as claims 11, 12, 14, 27, 28, 36, 37 and 42 are now in proper form and allowable over the cited references, favorable consideration and a notice of allowance are earnestly solicited.

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Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with Markings to Show Changes Made".

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 13, 29, 38 and 43 have been canceled.

Claims 11, 27, 36 and 42 have been amended as follows:

11. (Amended) A refresh controller for use in a dynamic random access memory ("DRAM") having a full density mode and a reduced density mode, the refresh controller comprising:

an oscillator generating a periodic clock signal;

a counter having a clock input terminal coupled to receive the clock signal, the counter having first and second stages the first of which increments at a faster rate than the second, the second stage of the being two stages from the first stage of the counter so that the second stage is incremented at one-quarter the rate of the first stage; and

a selector circuit coupled the first and second stages of the counter, the selector circuit being operable to couple the first stage of the counter to an output terminal in the full density mode and being operable to couple the second stage of the counter to the output terminal in the reduced density mode.

27. (Amended) A dynamic random access memory ("DRAM") comprising:

an array of memory cells arranged in rows and columns;

a column address latch structured to store a column address responsive to a column address strobe signal;

a column decoder coupled to the column address latch to receive the stored column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in a full density mode to generate the first enable signal responsive to a first state of a least significant bit of the row address and to generate the second enable signal responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in a reduced density mode regardless of the state of the least significant bit of the row address;

a data path coupled between the memory array and a data terminal; and

a refresh controller for refreshing at least some of the memory cells in the memory array responsive to a refresh trigger signal, the refresh controller comprising:

an oscillator generating a periodic clock signal;

a counter having a clock input terminal coupled to receive the clock signal, the counter having first and second stages the first of which increments at a faster rate than the second, the second stage of the counter being two stages from the first stage of the counter so that the second stage is incremented at one-quarter the rate of the first stage; and

a selector circuit coupled the first and second stages of the counter, the selector circuit being operable to couple the first stage of the counter to an output terminal in the full density mode and being operable to couple the second stage of the counter to the output terminal in the reduced density mode, the refresh trigger signal being generated responsive to the counter stage coupled to the output terminal by the selector circuit being incremented or decremented..

36. (Amended) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a dynamic random access memory, comprising:

an array of memory cells arranged in rows and columns;

a column address latch structured to store a column address responsive to a column address strobe signal;

a column decoder coupled to the column address latch to receive the stored column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in the full density mode to generate the first enable signal responsive to a first state of a least significant bit of the row address and to generate the second enable signal responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in a reduced density mode regardless of the state of the least significant bit of the row address;

a data path coupled between the memory array and a data terminal; and

a refresh controller for refreshing at least some of the memory cells in the memory array responsive to a refresh trigger signal, the refresh controller comprising:

an oscillator generating a periodic clock signal;

a counter having a clock input terminal coupled to receive the clock signal, the counter having first and second stages the first of which increments at a faster rate than the second, the second stage of the counter being two stages

from the first stage of the counter so that the second stage is incremented at one-quarter the rate of the first stage; and

a selector circuit coupled the first and second stages of the counter, the selector circuit being operable to couple the first stage of the counter to an output terminal in the full density mode and being operable to couple the second stage of the counter to the output terminal in the reduced density mode, the refresh trigger signal being generated responsive to the counter stage coupled to the output terminal by the selector circuit being incremented or decremented.

42. (Amended) A method of refreshing a dynamic random access memory ("DRAM") having a full density operating mode and a reduced density operating mode, the method comprising:

determining the operating mode of the DRAM;

if the DRAM is determined to be operating in the full density mode, refreshing the DRAM at a first rate; and

if the DRAM is determined to be operating in the reduced density mode, refreshing the DRAM at a second rate, the second rate being 8 times slower than the first rate.

